

Amendments to the Claims:

Claim 6 has been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

Claims 1-5. (Canceled)

6. (Currently Amended) A method of making a transistor on a substrate having a dielectric layer thereon comprising:
forming a gate structure overlying the dielectric layer, the gate structure having a gate oxide layer formed on said dielectric layer, and a metal silicide layer formed on said gate oxide layer, said gate structure having a first sidewall and a second sidewall defining a first contact region, a channel region and a second contact region therewithin;
forming first, second and third subregions within the second contact region, each subregion having a dopant concentration that different from that of the other two subregions, wherein forming said subregions comprises:
forming a first single thin layer sidewall spacer of dielectric material overlying said second sidewall, said first single thin layer sidewall spacer formed by depositing a thin conformal layer of dielectric material over said substrate and etching to a predetermined thickness over said second sidewall for an annealing/oxidation step at an elevated temperature;
introducing a first dopant into the substrate to form said first subregion, said first subregion being generally aligned with said second single layer sidewall spacer;

forming a second single layer sidewall spacer overlying said first single thin layer spacer,
said second single layer sidewall spacer having a thickness greater than said first
single thin layer sidewall spacer;
~~introducing a first dopant into the substrate to form said first subregion, said first~~
~~subregion being generally aligned with said second single layer sidewall spacer;~~
reducing the thickness of the second single layer sidewall spacer to form a third sidewall
spacer having a thickness intermediate said first and second sidewall spacers;
introducing a second dopant into the substrate to form said second subregion, said second
subregion being essentially ~~generally~~ aligned with the third sidewall spacer;
substantially removing the third sidewall spacer; and
introducing a third dopant into the substrate to form said third subregion, said third
subregion being essentially ~~generally~~ aligned with said second sidewall.

7. (Previously Presented) The method of claim 6, wherein the first single thin layer
sidewall spacer is anisotropically etched to a thickness of between about 50 and 150 Angstroms.

8. (Previously Presented) The method of claim 6, wherein the second single layer
sidewall spacer is etched to a thickness of about 2 to 20 times the thickness of said first single
thin layer sidewall spacer.

9. (Previously Presented) The method of claim 6, wherein the second single layer
sidewall spacer is etched to a thickness of about 550 Angstroms.

10. (Previously Presented) The method of claim 6, wherein said first single thin layer
sidewall spacer is formed of one of silicon nitride and silicon dioxide.